REMARKS

The Office Action dated September 27, 2004 has been received and reviewed. Claims 1-23 stand rejected. New claims 24-27 are being added by this amendment. Accordingly, claims 1-27 are presently in the application.

Claims 1-3, 8-11, 13, 18-21, and 23 stand rejected under 35 USC 103(a) as being unpatentable over Yasuda (US 6,081,347). Referring to Figure 2 of the Yasuda patent, Yasuda discloses a high-speed image bus 216 for inputting and outputting image data by establishing mutual connection between, *inter alia*, a RIP 205, an image processing unit 206, and a scanner interface 218 connected to a scanner (image input unit) 217 (col. 5, lines 45-54). The high speed image bus 216 is controlled as a singular component by a bus controller 222 to transfer data among the various other components. It is noteworthy that only one bus is disclosed for these purposes.

In contrast with Yasuda, the system according to the present invention (as shown in Figure 2 of the specification) includes an image processor 14 having a printer image data path that is separate from its printer control and status path. More specifically, the image processor 14 comprises a first processor system 30 and a second processor system 32 separately connected to an image source 12. The first processor system 30 is characterized by providing high-level control of the image processing performed within the image processor 14. The first processor system 30 also provides high-level control of image acquisition performed by the image processor 14, e.g., handshaking during image transfers from the image source 12 to the second processor system 32. Thus, the first processor system 30 coordinates or orchestrates control of image acquisition. The second processor system 32 is characterized by performing a majority of the image processing performed within the image processor 14 responsive to control by the first processor system 30. Furthermore, the second processor system 32 accepts and stores images from the image source 12, as coordinated by the first processor system 30 via a control/status bus 42.

More specifically, the first processor system 30 is in circuit communication with the image source 12 via *a first bus, referred to as a print*

control bus 34. The print control bus 34 can be a bus of virtually any protocol; since speed of transfer is not critical for the print control bus 34, a slower bus, although not required, may be used. The second processor system 32 is in circuit communication with the image source 12 via *a second bus, referred to as an image data bus 36*. Although virtually any bus protocol can be used for the image data bus 36, because image files can be very large, speed of transfer is important between the image source 12 and the second processor system 32 along that bus. Therefore, any of a number of known faster buses are preferred for the image data bus 36.

The advantage of the invention is that the separate processors and *separate bus paths* for printer image data and printer control and status data allow the system to minimize the "housekeeping" performed by the processor system performing the image processing, thereby streamlining image processing and increasing the speed of high-speed printing.

In claiming an image processor for generating image output for a printer from image data received from an image source, claim 1 recites two processor components and two bus configurations: (a) a first processor system, characterized by having *a first bus for communication with the image source*, where the first processor system communicates control data with the image source via the first bus... ; and (b) a second processor system in circuit communication with the first processor system and characterized by having *a second bus for communication with the image source*, where the second processor system receives image data from the image source via the second bus. The second processor system is further characterized by performing a majority of the image processing performed within the image processor *responsive to control by the first processor system* (italics added for purpose of these remarks). Independent claim 23 has similar limitations.

In rejecting claim 1, the Examiner alleges that Yasuda discloses an image processor comprising a first processor system (206) having a first bus for communication with the image source 217 and a second processor system (205) in circuit communication with the first processor system and having a second bus for communication with the image source. The bus in both cases is described as the bus connecting the respective processing system to the scanner interface 218.

Yasuda however clearly shows one and the same bus connecting the first processor system (image processing unit 206) and the second processing unit (RIP 205) to the scanner 217 via the scanner interface 218, namely, the high speed image bus 216 (col. 5, lines 45-49). In other words, for sake of argument, if the high speed image bus 216 is considered to be the "first bus" there is nothing in Yasuda showing any suggestion of a "second bus". Nor is there any need for providing a second bus, inasmuch as both processing units require the same high speed bus configuration for interconnecting with the image source, that is, the high speed image bus 216. Absent such need, any motivation for adding a second bus, for which speed of transfer is not critical, is completely missing.

Furthermore, Yasuda fails to disclose that the second processor performs image processing responsive to control by the first processor system, as noted above in the italicized portion of claim 1. Unlike applicants' system, where the first processor provides control data, both cited processors in Yasuda are processing image data – thus requiring the single high speed bus. Neither processor functions to provide control over the other. The Examiner acknowledges that Yasuda "does not directly teach that the second processor system 205 performs a majority of the image processing performed in the image processor *responsive to control by the first processor system 206*." (bottom page 2, italics added). While going on to argue that Yasuda indirectly discloses that processor 205 performs a majority of the image processing, the Examiner's argument fails to show how the second processor is "*responsive to control by the first processor system 206*" In fact, the "second processor" (RIP 205) is not responsive to control by the "first processor" (Image Processing Unit 206), and there is no reasonable suggestion or motivating influence for making it so.

It is respectfully suggested that a rejection under 35USC103(a) may not be maintained unless, among other requirements, (1) all of the claim limitations are taught or suggested by the prior art, and (2) there is some suggestion or motivation in the first place to draw upon the cited prior art, such that each claim limitation is taught or suggested in the prior art. These are among the requirements for a *prima facie* case of obviousness. MPEP 2143.01 – 2143.03. Yasuda fails to show any suggestion or motivation for minimizing the "housekeeping" performed by the processor system by enhancing the disclosed

bus with the connection of an additional bus to an image source for providing high level control, and is further silent as to any suggestion for having one processor responsive to control by the other processor. Accordingly, the rejection of pending claims 1-3, 8-11, 13, 18-21, and 23 does not meet the aforementioned requirements, either wholly or in part, and is accordingly traversed.

In rejecting claims under 35 U.S.C. §103(a), the Examiner bears the initial burden of presenting a *prima facie* case of obviousness. *In re Oetiker, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).* Only if that burden is met does the burden of coming forward with evidence or argument shift to the applicant. *Id.* "A *prima facie* case of obviousness is established when the teachings from the prior art itself would appear to have suggested the claimed subject matter to a person of ordinary skill in the art." *In re Bell, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993)* quoting *In re Rinehart, 189 USPQ 143, 147 (CCPA 1976).* If the Examiner fails to establish a *prima facie* case, the rejection is improper and will be overturned. *In re Fine, 5USPQ2d 1596, 1598 (Fed. Cir. 1988).* For reasons as set forth above, the Examiner has not established a *prima facie* case, and the claims 1-3, 8-11, 13, 18-21, and 23 therefore should be in allowable condition as they stand.

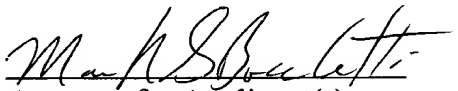
Claims 4-7, 12, 14-17 and 22 stand rejected under 35 USC 103(a) as being unpatentable over Yasuda as applied to claims 1-3 and further in view of Clark (US 5,899,604). Claim 4-7, 12, 14-17 and 22 are dependent on claim 1, and therefore include all the features thereof. Accordingly, for the reasons set forth above with regard to claim 1, claims 4-7, 12, 14-17 and 22 are also believed to be patentable.

New claims 24-27 have been added to claim a further recitation of the invention. Furthermore, claim 14 has been amended to depend from claim 24, such that original claims 15-22 now also depend from new claim 24 (via claim 14). Support for the language in new claim 24 regarding the respective printer image data path and the printer control and status path can be found on page 7, lines 3-5 of the application and the print control bus and the image data bus is found on page 8, lines 12-19. The control/status bus 42 recited in claim 25 is found on page 9, lines 16-18.

The remaining references – Cyman et al. (US Patent No. 6,236.463) and Clouthier (US Patent No. 6,778,291) – were not relied upon by the Examiner on their merits in relation to the claims but merely considered pertinent to applicant's disclosure. They have been considered for purposes of this response but are at most cumulative and not believed to be otherwise relevant.

For the reasons set forth above, it is believed that the application is in condition for allowance. Accordingly, reconsideration and favorable action are respectfully requested.

Respectfully submitted,



Attorney for Applicant(s)
Registration No. 31,330

Mark G. Bocchetti/gms
Rochester, NY 14650
Telephone: 585-477-3395
Facsimile: 585-477-4646

If the Examiner is unable to reach the Applicant(s) Attorney at the telephone number provided, the Examiner is requested to communicate with Eastman Kodak Company Patent Operations at (585) 477-4656.